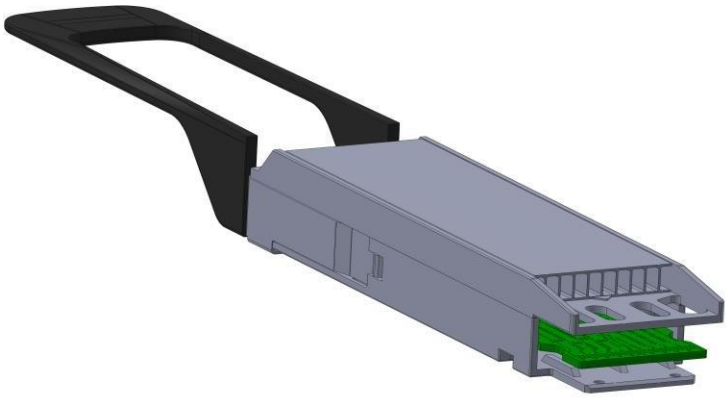
ML4064-LB Rev2

OSFP Electrical Passive Loopback Module



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ML4064-LB OSFP 8x50G Passive Loopback Modules - Key Features

- ✓ Loops back TX & RX with good performance SI Traces
- ✓ Built with advanced PCB Material (Rogers/Megtron)
- ✓ MSA Compliant Shell with latching mechanism
- ✓ Nine thermal spots
- ✓ Can emulate all 5 OSFP power classes
- ✓ Can dissipate up to 16W via the thermal loads
- ✓ Temp sense
- ✓ I2C Terminated by microcontroller, I2C slave compliant with MSA
- ✓ Implements MSA Memory Map with programmable new pages
- ✓ Ability to control/ monitor all low speed signals
- ✓ Insertion Counter
- ✓ Front LED Indicator
- ✓ Hot Pluggable
- ✓ Cut-off temperature preventing module overheating
- ✓ AC-coupled High Speed Interface

LED Indicator

Green (Solid) - Signifies that the module is operating in high power mode.
Red (Solid) - Signifies the module is operating in low power mode.
Green/Red (Blinking) - Signifies that an alarm is asserted.

Operating Conditions

Recommended Operation Conditions						
Parameter	**Symbol**	**Notes/Conditions**	**Min**	**Typ**	**Max**	**Units**
Operating Temperature	T_A		0		85	°C
Supply Voltage	VCC	Main Supply Voltage	2.97	3.3	3.63	V
Data Rate	R_b	Guaranteed to work at 50 Gbps per lane	0		400	Gbps
Input/Output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0		16	W

1. General Description

The ML4064-LB is an OSFP passive electrical loopback module which is a hot pluggable form factor designed for high speed testing application for OSFP host ports. The ML4064-LB is designed for 400 Gigabit Ethernet applications and provides 8x50G RX and TX lanes, I2C module management interface and all the OSFP SFF hardware signals.

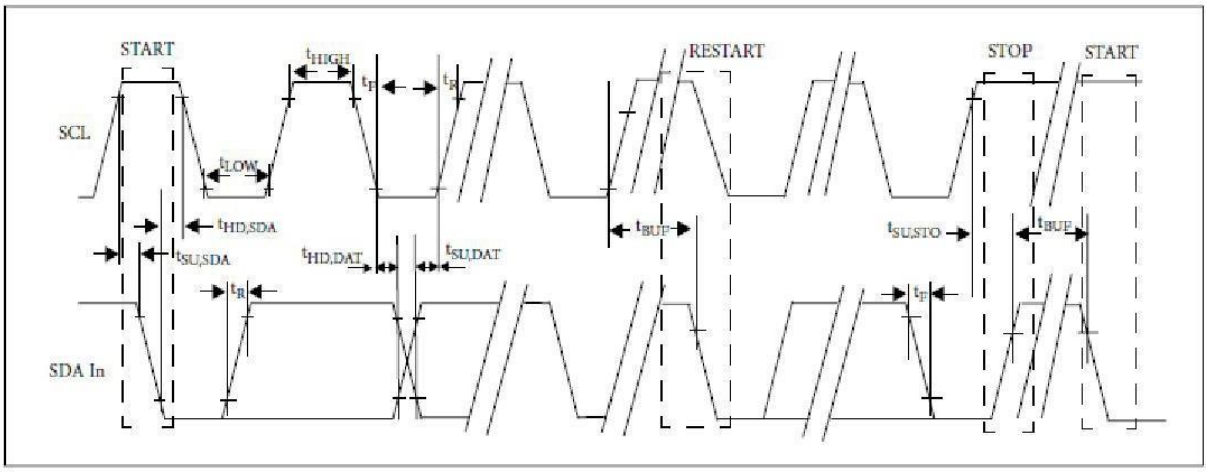
The ML4064-LB loops back 8-lane 50Gb/s transmit data from the Host back to 8-lane 50Gb/s receive data port to the Host.

The ML4064-LB provides programmable power dissipation up to 16W allowing the module to emulate all the OSFP power classes. It also provides an insertion counter, a LED blinking rate, an upper temperature cut-off and a temperature sensor.

2. Functional Description

2.1 I2C Signals, Addressing and Frame Structure

I2C Frame:



Before initiating a 2-wire serial bus communication, the host shall provide setup time on the ModSelL line of all modules on the 2-wire bus. The host shall not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied. The 2-wire serial interface address of the OSFP module is 1010000X (A0h). In order to allow access to multiple OSFP modules on the same 2-wire serial bus, the OSFP pinout includes a ModSelL or module select pin. This pin (which is pulled high or deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}	0.03	1	MHz
Clock Pulse Width Low	t_{LOW}	1.2		us
Clock Pulse Width High	t_{High}	1.1		us
Time bus free before new transmission can start	t_{BUF}	20.8		us
Input Rise Time (400kHz)	$t_{R,400}$	300		ns
Input Fall Time (400kHz)	$t_{F,400}$	300		ns
ModSelL Setup Time	Host_select_setup	2		ms
ModSelL Hold Time	Host_select_hold	10		us
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	us

Maximum time the OSFP Module may hold the SCL line low before continuing with a read or write operation is 500us.

2.1.1 Device Addressing and Operation

Serial Clock (SCL): The host supplied SCL input to OSFP transceivers is used to positive-edge clock data into each OSFP device and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven.

Master/Slave: OSFP transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: Each OSFP is hard wired at the device address A0h.

Multiple Devices per SCL/SDA: While OSFP transceivers are compatible with point-to-point SCL/SDA, they can share a single SCL/SDA bus by using the OSFP ModSelL line.

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicating a START or STOP condition. All addresses and data words are serially transmitted to and from the OSFP in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host shall be acknowledged by OSFP transceivers. Read data bytes transmitted by OSFP transceivers shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the OSFP management interface can be reset. Memory reset is intended only to reset the OSFP transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1. Clock up to 9 cycles
2. Look for SDA high in each cycle while SCL is high
3. Create a Start condition as SDA is high

Device Addressing: OSFP devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 1. This is common to all OSFP devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 1: OSFP Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address (with ModSelL in the low state) the OSFP transceiver shall output a zero (ACK) on the SDA line to acknowledge the address.

2.2 I2C Read/Write Functionality

2.2.1 OSFP Memory Address Counter (Read AND Write Operations)

OSFP devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the module. This address stays valid between operations as long as OSFP power is maintained. The address “roll over” during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

2.2.2 Read Operations

A. Current Address Read

A current address read operation requires only the device address read word (10100001) be sent, see Figure 2 below.

		<-- QSFP+ ADDRESS --->																		
HOST	START	MSB						LSB	READ									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
QSFP+										ACK	MSB							LSB		
											<---- DATA WORD ----->									

Figure 2: OSFP Current Address Read Operation

Once acknowledged by the OSFP, the current address data word is serially clocked out. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

B. Random Read

A random read operation requires a “dummy” write operation to load in the target byte address as shown in Figure 3 below. This is accomplished by the following sequence.

		<- QSFP+ ADDRESS ->									<- MEMORY ADDRESS ->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
QSFP+										ACK									ACK

	<- QSFP+ ADDRESS ->																	
START	MSB						LSB	READ									NACK	STOP
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
									ACK	MSB							LSB		
										<---- DATA WORD n---->									

Figure 3: OSFP Random Read

The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the OSFP. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The OSFP acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

C. Sequential Read

Sequential reads are initiated by a current address read (Figure 4). To specify a sequential read, the host responds with an acknowledgement (instead of a STOP) after each data word. As long as the OSFP receives an acknowledgement, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledgement.

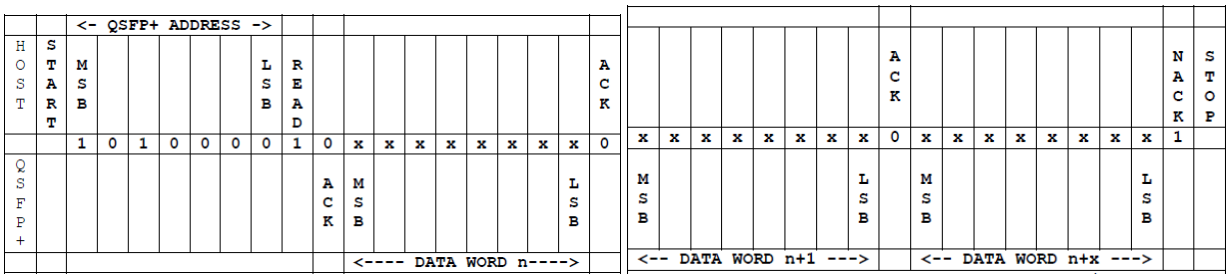


Figure 4: Sequential Address Read Starting at OSFP Current Address

2.3 Low-Speed Signals

2.3.1 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module.
Reset is an active low signal on the host which is translated to an active low signal on the module.
Interrupt is an active high signal on the module which gets translated to an active low signal on the host.

2.3.2 LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present.
Low Power mode is an active low signal on the host which gets converted to an active low signal on the module.
Module Present is controlled by a pull down resistor on the module which gets converted to an active low logic signal on the host.

2.4 ML4064-LB Specific Functions

2.4.1 Temperature Sensor

The ML4064-LB has two internal temperature sensors (top and bottom) in order to continuously monitor the module temperature. The temperature sensor values for top case readings are present in low-memory registers 14-15 and for the bottom are in registers 12-13. Internally measured Module

temperature are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius. Temperature accuracy is better than ±1 degrees Celsius over specified operating temperature and voltage.

Address	Bit	Name	Description
12	ALL	Temperature 2 MSB	Internally measured module temperature (Bottom)
13	ALL	Temperature 2 LSB	Internally measured module temperature (Bottom)
14	ALL	Temperature 1 MSB	Internally measured module temperature (Top)
15	ALL	Temperature 1 LSB	Internally measured module temperature(Top)

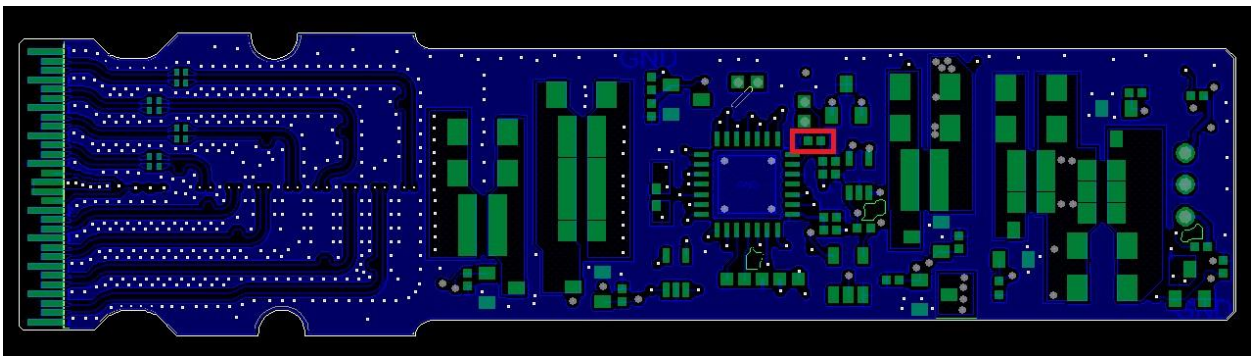


Figure 5- Top Temperature Sensor

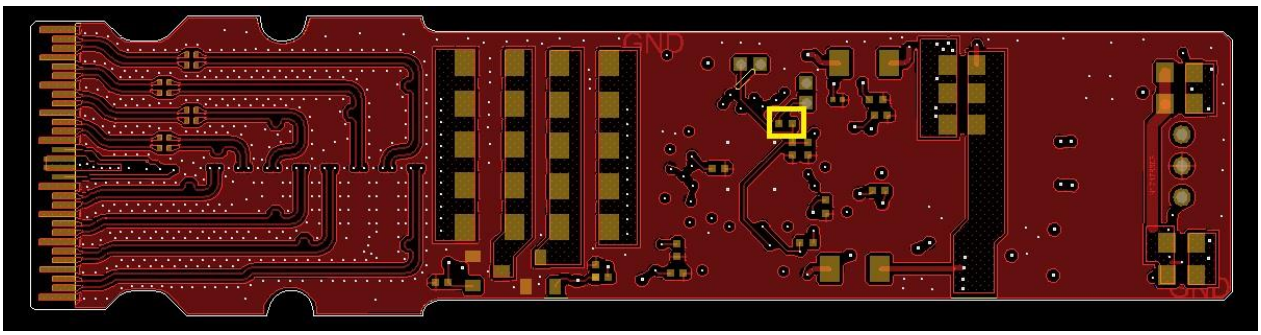


Figure 6-Bottom Temperature Sensor

In upper page 02 exists the thresholds of the temperature alarms and warnings.

Address	Page	Bit	Name	Description	Type	Default Value	Decimal
128	Page 02	ALL	Temp_Alarm_High_MSB	Thresholds for internally measured temperature monitor: signed 2's complement in 1/256 degree Celsius increments	RW	0x50	80◦C
129		ALL	Temp_Alarm_High_LSB		RW	0x00	
130		ALL	Temp_Alarm_Low_MSB		RW	0x00	0◦C
131		ALL	Temp_Alarm_Low_LSB		RW	0x00	
132		ALL	Temp_War_High_MSB		RW	0x4B	75◦C
133		ALL	Temp_War_High_LSB		RW	0x00	
134		ALL	Temp_War_Low_MSB		RW	0x05	5◦C
135		ALL	Temp_War_Low_LSB		RW	0x00	

2.4.2 Voltage Sense

A voltage sense circuit is available allowing the measure of internal module supplied voltage Vcc. Supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 – 65535) in increments of 100 µV, yielding a total measurement range of 0 to +6.55 Volts.

Address	Bit	Name	Description
16	ALL	Supply 3.3-volt MSB	Internally measured module temperature
17	ALL	Supply 3.3-volt LSB	Internally measured module temperature

In upper page 02 exists the thresholds of the Voltage alarms and warnings.

Address	Page	Bit	Name	Description	Type	Init Value	Decimal
136	Page 02	ALL	VCC_Alarm_High_MSB	Thresholds for internally measured 3.3 volt input supply voltage: in 100 uV increments	RW	0x8D	3.63V
137		ALL	VCC_Alarm_High_LSB		RW	0xCC	
138		ALL	VCC_Alarm_Low_MSB		RW	0x74	2.97V
139		ALL	VCC_Alarm_Low_LSB		RW	0x04	
140		ALL	VCC_War_High_MSB		RW	0x8B	3.58V
141		ALL	VCC_War_High_LSB		RW	0xD8	
142		ALL	VCC_War_Low_MSB		RW	0x75	3.02V
143		ALL	VCC_War_Low_LSB		RW	0xF8	

2.4.3 Insertion Counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved, and can be read anytime from registers 248 and 249 from Page 03.

Address	Page	Bit	Name	Description	Type	Default Value
248	Page 03	LSB	Insertion Counter MSB	LSB unit = 1 insertion	RO	0x00
249		MSB	Insertion Counter LSB		RO	0x00

2.4.4 Programmable Power Dissipation & Thermal Emulation

In upper **Page 00**, bit 0 of register 200 determines the power up of the module. The default value is 0 referring to Custom Power Mode. The power class identifier is selected when the value is 1.

Address	Page	Bit	Description	Type	Default Value
200	Page 00	0	Power up Selection	RW	0

A. Custom Power Mode

The consumed power changes accordingly when the value in this register is changed (only when in high power mode). In Low power mode the module automatically turns off PWM. In addition to the PWM Registers, there's static power spots for controlling the power. The values written in this register are permanently stored. The PWM can also be used for module thermal emulation. All registers are in upper page 03.

Address	Page	Bit	Name	Description	Type	Default Value
251	Page 03	ALL	PWM1	Control PWM1 (bottom 1.94W spot) Range: 0-255 (PWM signal)	RW	0x00
252		ALL	PWM2	Control PWM2 (bottom 1.45W spot) Range: 0-255 (PWM signal)	RW	0x00

Address	Page	Bit	Name	Description	Type	Default Value
250	Page 03	6	Static Power Spots	Control PWM5 (bottom 1.45W spot) 0: disable 1: enable	RW	0x00
		5		Control PWM8 (bottom 1.8W spot) 0: disable 1: enable		
		4		Control PWM7 (top 1.94W spot) 0: disable 1: enable		

		3		Control PWM6 (top 1.94W spot) 0: disable 1: enable		
		2		Control PWM5 (top 1.94W spot) 0: disable 1: enable		
		1		Control PWM4 (top 3W spot) 0: disable 1: enable		
		0		Control PWM3 (top 1.94W spot) 0: disable 1: enable		

B. Power Class

The power class identifier specifies maximum power dissipation, when selecting a power class the module operates at its maximum power.

Address	Page	Bit	Name	Type	Description
200	Page 00	7-5	Module Card Power Class	RW	000: Power class 1 (2 W maximum) 001: Power class 2 (4 W maximum) 010: Power class 3 (8 W maximum) 011: Power class 4 (12 W maximum) 100: Power class 5 (16 W maximum)
		4-1	Reserved		
		0	Power up selection	RW	0: PWM 1:Power Class

2.4.5 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.

The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, the PWM will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM goes back to its previous value.

The Cut-Off temperature for the ML4064-LB is 85˚C and it can be programmed to any value from register 253 of memory page 03. The Max Value that can be written is 90◦C.

Address	Page	Bit	Name	Description	Type	Default Value
253	Page 03	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 degC	RW	0x55(85◦C)

2.4.6 Low speed signals pin status

Name	Page	Address	Bit	Description	Type
LPWn/PRSn	Page 03	254	1	1: high 0: low	RO
LPWn pin state transition		254	4	Read 0b: No edge detected Read 1b: Either rising edge or falling edge crossing the 1.25V .Threshold is detected Write 0b: No effect Write 1b: Clear the register	RW

All these registers are accessed from memory page 03.

2.4.7 INTL Control

During power-up of the module, INT is defaulted to negated. Afterward, host can set the status of this indicator to any status through an I2C registers **in upper page 03**. Setting it should not affect any operation in the module.

Address	Bit	Name	Description	Type
255	1-0	INTL_CNT	Digital Control of INT 00: Normal Operation 10: Force the INTL to logic 0 11: Force the INTL to logic 1	RW

For “Normal Operation”, the INTL is asserted when the alarm or warning is high (VCC or Temperature) and the LED will start blinking. If the INTL_CNT is set from this register, the LED won’t blink.

Revision History

Revision number	Date	Description
0.1	27/07/2017	▪ Preliminary
0.2	16/08/2017	▪ Added parag 2.1, 2.2, 2.3 ▪ Typo in Operating Conditions
0.3	6/1/2018	▪ Added parag 2.4.5, 2.4.7 ▪ Update parag 2.4.1, 2.4.2, 2.4.3, 2.4.4